

CLAIM AMENDMENTS:

Please amend the claims as described below. In accordance with 37 CFR §1.121, a complete listing of all claims in the application is provided below. Notably, the status of each claim is indicated in the parenthetical expression adjacent to the claim number.

Claims 1 - 27 (**canceled**).

28. (**new**): A semiconductor memory array comprising:

a plurality of memory cells arranged in a matrix of rows and columns, the plurality of memory cells include a first memory cell and a second memory cell, wherein the first and second memory cells each include at least a transistor to constitute the memory cell and wherein the transistor includes:

a source region;

a drain region;

a body region disposed between and adjacent to the source region and the drain region, wherein the body region is electrically floating; and

a gate spaced apart from, and capacitively coupled to, the body region;

wherein each memory cell includes:

a first data state representative of a first charge in the body region; and

a second data state representative of a second charge in the body region

wherein the second charge is substantially provided by removing charge from the body region through the source region; and

wherein the drain region of the first memory cell and the drain region of the second memory cell are the same region.

1 29. **(new)**: The memory array of claim 28 wherein the plurality of memory cells
2 further includes a third memory cell wherein the third memory cell includes at least a
3 transistor to constitute the memory cell and wherein the transistor includes:

4 a source region;

5 a drain region;

6 a body region disposed between and adjacent to the source region and the
7 drain region, wherein the body region is electrically floating; and

8 a gate spaced apart from, and capacitively coupled to, the body region;

9 wherein each memory cell includes:

10 a first data state representative of a first charge in the body region; and

11 a second data state representative of a second charge in the body region

12 wherein the second charge is substantially provided by removing charge from the
13 body region through the source region; and

14 wherein the source region of the second memory cell and the source region of the
15 third memory cell are the same region.

1 30. **(new)**: The memory array of claim 28 further including a control unit, coupled to
2 the gate and the drain region of the first memory cell, to provide control signals to the first
3 memory cell, wherein the first memory cell, in response to a first write control signal set,
4 stores the first charge in the body region and wherein the first charge is comprised of an
5 accumulation of majority carriers in the body region.

1 31. **(new)**: The memory array of claim 30 wherein the majority carriers accumulate
2 in a portion of the body region that is adjacent to the source region of the first memory cell

3 and wherein the source regions of the first and second memory cell are connected to a
4 fixed voltage.

1 32. **(new)**: The memory array of claim 28 further including a control unit, coupled to
2 the gate and the drain region of the first memory cell, to provide control signals to the first
3 memory cell, wherein the first memory cell, in response to a second write control signal set,
4 stores the second charge in the body region wherein the second charge is substantially
5 provided by removing charge from the body region through the source region.

1 33. **(new)**: The memory array of claim 32 wherein the second write control signal
2 set includes at least first and second signals having positive voltages wherein the first
3 signal is applied to the drain region of the first memory cell and the second signal is applied
4 to the gate of the first memory cell.

1 34. **(new)**: The memory array of claim 28 further including:
2 a reading unit, coupled to the drain region of the first memory cell, to determine the
3 data state of the first memory cell;
4 a control unit, coupled to gate of the first memory cell, to provide control signals to
5 the first memory cell; and
6 wherein, in response to a read control signal applied to the gate of the first memory
7 cell, the reading unit determines the charge stored in the body region of the first memory
8 cell.

1 35. **(new)**: A semiconductor memory array comprising:

2 a plurality of memory cells arranged in a matrix of rows and columns, the plurality of
3 memory cell include a first memory cell and a second memory cell, wherein the first and
4 second memory cells each include at least a transistor to constitute the memory cell and
5 wherein the transistor includes:

6 a source region having impurities to provide a first conductivity type;

7 a drain region having impurities to provide the first conductivity type,

8 a body region disposed between and adjacent to the source region and the
9 drain region wherein the body region is electrically floating and includes impurities to
10 provide a second conductivity type wherein the second conductivity type is different
11 than the first conductivity type;

12 a gate disposed over the body region;

13 wherein the memory cell includes:

14 a first data state representative of a first charge in the body region wherein
15 the first charge is substantially provided by impact ionization; and

16 a second data state representative of a second charge in the body region
17 wherein the second charge is substantially provided by removing charge from the
18 body region through the source region; and

19 wherein the drain region of the first memory cell and the drain region of the second
20 memory cell are the same region.

1 36. **(new)**: The memory array of claim 35 wherein the plurality of memory cells
2 further includes a third memory cell wherein the third memory cell includes at least a
3 transistor to constitute the memory cell and wherein the transistor includes:

4 a source region having impurities to provide a first conductivity type;
5 a drain region having impurities to provide the first conductivity type,
6 a body region disposed between and adjacent to the source region and the
7 drain region wherein the body region is electrically floating and includes impurities to
8 provide a second conductivity type wherein the second conductivity type is different
9 than the first conductivity type;
10 a gate disposed over the body region;
11 wherein the memory cell includes:
12 a first data state representative of a first charge in the body region wherein
13 the first charge is substantially provided by impact ionization; and
14 a second data state representative of a second charge in the body region
15 wherein the second charge is substantially provided by removing charge from the
16 body region through the source region; and
17 wherein the source region of the second memory cell and the source region of the
18 third memory cell are the same region.

1 37. **(new)**: The memory array of claim 35 further including a control unit, coupled to
2 the gate and drain region of the first memory cell, to apply control signals to the first
3 memory cell wherein the control signals include a first write control signal set to accumulate
4 the first charge in the body of the first memory cell and a second write control signal set to
5 provide the second charge in the body region by removing charge from the body region
6 through the source region.

1 38. **(new)**: The memory array of claim 37 wherein the first charge is stored in the
2 body region of the first memory cell in response to applying a first signal, having a first
3 negative voltage, to the drain region and a second signal, having a second negative
4 voltage, to the gate.

1 39. **(new)**: The memory array of claim 38 wherein the first memory cell stores at
2 least a substantial portion of the first charge in a portion of the body region of the first
3 memory cell that is adjacent to the source region of the first memory cell.

1 40. **(new)**: The memory array of claim 37 wherein the second write control signal
2 set includes a first signal, having a first positive voltage, applied to the drain region of the
3 first memory cell and a second signal, having a second positive voltage, applied to the gate
4 of the first memory cell.

1 41. **(new)**: The memory array of claim 40 wherein the source regions of the first
2 and second memory cells are connected to a fixed voltage.

1 42. **(new)**: The memory array of claim 41 wherein the second charge is stored in
2 the body region in response to removing the first positive voltage from the drain region of
3 the first memory cell before removing the second positive voltage from the gate of the first
4 memory cell.

1 43. **(new)**: The memory array of claim 42 wherein, in response to the first and
2 second positive voltages, the first memory cell includes a forward bias current between its
3 body region and its source region.

1 44. **(new)**: The memory array of claim 43 wherein the second charge is stored in
2 the body region of the first memory cell in response to removing the first positive voltage
3 from the drain region of the first memory cell and the second positive voltage from the gate
4 of the first memory cell.

1 45. **(new)**: The memory array of claim 35 further including:
2 a reading unit, coupled to the drain region of the first memory cell, to determine the
3 data state of the first memory cell;
4 a control unit, coupled to gate of the first memory cell, to provide control signals to
5 the first memory cell; and
6 wherein, in response to a read control signal applied to the gate of the first memory
7 cell, the reading unit senses the charge stored in the body region of the first memory cell.

1 46. **(new)**: The memory array of claim 37 wherein the second write control signal
2 set includes a first signal, having a first positive voltage, applied to the drain region of the
3 first memory cell.

1 47. **(new)**: The memory array of claim 46 wherein the second charge is stored in
2 the body region in response to removing the first positive voltage from the drain region of

3 the first memory cell before removing the second positive voltage from the gate of the first
4 memory cell.

1 48. **(new)**: The memory array of claim 47 wherein, in response to the first and
2 second positive voltages, the first memory cell includes a forward bias current between its
3 body region and its source region.

1 49. **(new)**: The memory array of claim 48 wherein the second charge is stored in
2 the body region of the first memory cell in response to removing the first positive voltage
3 from the drain region of the first memory cell and wherein the source regions of the first and
4 second memory cells are connected to a fixed voltage.

1 50. **(new)**: A semiconductor memory array comprising:
2 a plurality of memory cells, arranged in a matrix of rows and columns, including a
3 first memory cell and a second memory cell, wherein the first and second memory cells
4 each include at least a transistor to constitute the memory cell and wherein the transistor
5 includes:

6 a source region having impurities to provide a first conductivity type;

7 a drain region having impurities to provide the first conductivity type,

8 a body region disposed between and adjacent to the source region and the

9 drain region wherein the body region is electrically floating and includes impurities to

10 provide a second conductivity type wherein the second conductivity type is different

11 than the first conductivity type;

12 a gate spaced apart from, and capacitively coupled to, the body region,
13 wherein the memory cell includes:
14 a first data state representative of a first charge in the body; and
15 a second data state representative of a second charge in the body region
16 wherein the second charge is substantially provided by removing charge from the
17 body region through the source region; and
18 wherein the drain region of the first memory cell and the drain region of the second
19 memory cell are the same region.

1 51. **(new)**: The memory array of claim 50 wherein the plurality of memory cells
2 further includes a third memory cell wherein the third memory cell includes at least a
3 transistor to constitute the memory cell and wherein the transistor includes:
4 a source region having impurities to provide a first conductivity type;
5 a drain region having impurities to provide the first conductivity type,
6 a body region disposed between and adjacent to the source region and the drain
7 region wherein the body region is electrically floating and includes impurities to provide a
8 second conductivity type wherein the second conductivity type is different than the first
9 conductivity type;
10 a gate spaced apart from, and capacitively coupled to, the body region;
11 wherein the memory cell includes:
12 a first data state representative of a first charge in the body; and
13 a second data state representative of a second charge in the body region
14 wherein the second charge is substantially provided by removing charge from the
15 body region through the source region; and

16 wherein the source region of the second memory cell and the source region of the
17 third memory cell are the same region.

1 52. **(new)**: The memory array of claim 50 further including a control unit, coupled to
2 the first memory cell, to control the data state of the first memory cell wherein, in response
3 to a first voltage applied to the drain region of the first memory cell and a second voltage
4 applied to the gate of the first memory cell, the first charge is removed from the body region
5 of the first memory cell through its source region.

1 53. **(new)**: The memory array of claim 52 wherein the control unit, in response to
2 removing the first voltage from the drain region of the first memory cell before removing the
3 second voltage from the gate of the first memory cell, causes the second charge to be
4 stored in the body region of the first memory cell.

1 54. **(new)**: The memory array of claim 52 wherein the control unit, in response to
2 applying ground to the drain region of the first memory cell before removing the second
3 voltage from the gate of the first memory cell, causes the second charge to be stored in the
4 body region of the first memory cell.

1 55. **(new)**: The memory array of claim 52 wherein the control unit, in response to
2 applying a third voltage to the drain region of the first memory cell before applying a fourth
3 voltage to the gate of the first memory cell, causes the first memory cell to store the second
4 charge in its body region.

1 56. **(new)**: The memory array of claim 52 wherein the first memory cell stores the
2 first charge in a portion of its body region that is adjacent to its source region.

1 57. **(new)**: The memory array of claim 52 further including a control unit, coupled to
2 the gate and the drain region of the first memory cell, to apply control signals to the first
3 memory cell wherein:

4 in response to a first write control signal set, the first memory cell generates and
5 stores the first charge in the body region; and

6 in response to a second write control signal set, the first memory cell generates and
7 stores the second charge in the body region wherein the first memory cell generates the
8 second charge by removing charge from its body region through its source region; and

9 wherein the first and second write control signal sets each include a plurality of
10 signals.

1 58. **(new)**: The memory array of claim 57 wherein the first write control signal set
2 includes a first signal having a first negative voltage to the drain and a second signal having
3 a second negative voltage to the gate and wherein, in response to the first and second
4 negative voltages, the first charge is stored in the body region of the first memory cell.

1 59. **(new)**: The memory array of claim 57 wherein the first memory cell stores the
2 first charge in a portion of the body region of the first memory cell that is adjacent to the
3 source region of the first memory cell.

1 60. **(new)**: The memory array of claim 57 wherein the second write control signal
2 set includes a first signal having a first positive voltage applied to the drain region and a
3 second signal having a second positive voltage applied to the gate.

1 61. **(new)**: The memory array of claim 60 wherein the second charge is stored in
2 the body region in response to removing the first positive voltage from the drain region of
3 the first memory cell before removing the second positive voltage from the gate of the first
4 memory cell.

1 62. **(new)**: The memory array of claim 61 wherein, in response to the first and
2 second positive voltages, the first memory cell includes a forward bias current between its
3 body region and the source region.

1 63. **(new)**: The memory array of claim 62 wherein the second charge is stored in
2 the body region of the first memory cell in response to removing the first positive voltage
3 from the drain region of the first memory cell and the second positive voltage from the gate
4 of the first memory cell.

1 64. **(new)**: The memory array of claim 50 further including:
2 a reading unit, coupled to the drain region of the first memory cell, to determine the
3 data state of the first memory cell;
4 a control unit, coupled to gate of the first memory cell, to provide control signals to
5 the first memory cell; and

6 wherein, in response to a read control signal applied to the gate of the first memory
7 cell, the reading unit senses the charge stored in the body region of the first memory cell.